## REMARKS

In response to the final Official Action of December 28, 2006, minor amendment has been made to the specification at page 3, line 25 to correct a grammatical error and claims 24, 35 and 42 have been amended in order to overcome the objections raised at Section I of the final Official Action. Claims 24, 41, 42 and 45 have been amended to make clear one feature of the present invention; namely, that in the case of sole addressing and accessing data, the access controllers provide access to the memory access by control ports and address ports of only one of the terminals. Support for this amendment is found in the original specification and drawings, including page 10, lines 1-5. Claim 46 has been amended to correct its dependency to claim 45.

Referring now to Section II, paragraph 6 rejects claims 24, 28-43 and 45 as anticipated in view of US patent 6,167,487, Camacho et al (hereinafter Camacho). For the reasons set forth below, this rejection is respectfully requested.

More particularly, the present invention relates to a memory unit having at least two memory areas for storing data. The memory areas may be accessed through two different terminals. Each of the terminals provides for address ports, control ports and data ports. By means of at least two access controllers, it is possible to selectively address and access data through the terminals individually or as a whole through one of the terminals. This means that the at least two access controllers allow accessing the data either through one of the terminals or through each of the terminals individually. In the case of sole addressing and accessing the data, the access controllers provide access to the memory areas by control ports and address ports of only one of the terminals and provide the data through data ports of both terminals. This feature allows for a lower clock frequency to be used which thereby reduces signal integrity issues.

According to Camacho, it is known to access a memory device through two different ports using a multi-port RAM-chip (MPRAM, see Camacho column 1, lines 35-55). Each of the ports provides for a dedicated, independent data path (see Camacho column 2, lines 20-23). It has been found that combining the data paths may be possible (see Camacho column 2, lines 46-54). The ports, which may be used

independently (see Camacho column 4, lines 26-28), may have address, control and data pins (see Camacho column 3, line 65 through column 4, line 3; column 5, lines 50-60). In a single mode, a user is enabled to combine the two ports into a single 32-bit port. This arrangement provides for a unified-port mode (see Camacho column 7, lines 32-38).

According to the present invention, in the case of sole addressing and accessing the data, the access controllers provide access to the memory areas by control ports and address ports of only one of the terminals. Using the address ports of only one of the terminals, data through the data ports of both terminals may be accessed and thus full data bus width is possible. Furthermore, as set forth at page 3, lines 15-25 of the present application, the present invention as claimed provides for data bus width in single mode which may be broader than in dual mode since in dual mode the data bus width has to be shared by at least two terminals whereas in single mode, only one terminal may use the whole data bus. However, as noted at the cited location, when in single mode not the whole bus width need be used. By providing this feature, support older memory architectures is provided. Since Camacho does not provide for accessing the memory used in the full data bus width as is possible with the present invention, a person skilled in the art would be led away from use of only one of the terminals as specified in each of the independent claims of the present application. Thus, in contrast to this feature of claim 24, Camacho proposes that access to data is possible through both control and address pins of both ports in combination (see Camacho column 7, lines 42-46). In the final Official Action, the Office relies on column 7, lines 33-56 with respect to a unified-port mode of operation. However, in this unified-port mode of operation, access to data is possible through both control and address pins of both ports in combination, in contrast to the method of the present invention as claimed in claim 24. That is, Camacho does not provide for accessing the memory using the full data bus width.

More particularly, Camacho discloses at column 7, lines 33-50 that to access the memory with a unified-port mode of operation, port A and port B provide external control and address signals so as to perform a single 32-bit write or read access (see Camacho

column 7, lines 39-43). Further, it is explained that address signals (ADA) through address pins of port A and address signals (ADB) through address pins of port B are provided. These two address signals ADA and ADB imply that for accessing the data, both ports/terminals provide address signals on their respective address pins. It is therefore believed not to be correct that this portion of Camacho discloses accessing the memory through the control and address ports of only one terminal and data ports of both terminals. In contrast, on port A, the address pins are provided with ADA and on port B, the address pins are provided with ADB. Thus, both address pins of both terminals are used in the unified-port mode as disclosed in Camacho.

Furthermore, when one port is disabled, the data pins of this port may not be used according to Camacho (see Camacho column 7, lines 50-56). This means that Camacho does not provide for accessing the memory using the full data bus-width, with the data pins of both terminals, through addressing and controlling the memory by only one port. In contrast, according to Camacho, the multi-port RAM (MPRAM) enables 16-bit, as well as 32-bit read and write access to the SRAM (see Camacho column 7, lines 51-52). As an additional feature, not being combined with the unified-port mode, Camacho further provides if one port of the MPRAM is disabled, the MPRAM would be fully functional via the other port. However, if one port is disabled, this port cannot provide data on its data pins. In short, if it is disabled, it is not possible to use its pins.

Therefore, accessing the whole memory through only one port, as disclosed in Camacho (see Camacho column 7, lines 54-56), does not disclose using data pins on both ports, but only that address signals ADA and ADB may locate any portion within the memory. The data is read from or written to this location using the data pins of the respective port and not the data pins of both ports. In view of these observations, it is respectfully submitted that claim 24, as amended, is not anticipated by Camacho.

Similar amendment has been made to independent claims 41, 42 and 45 and for similar reasons as those presented above, each of these claims is believed to be not anticipated by Camacho.

Since each of the independent claims is believed to be not anticipated by Camacho, it is respectfully submitted that all of the dependent claims thereto are further

not anticipated by Camacho, including those specifically rejected as anticipated at paragraph 6 of the Official Action; namely, claims 28-40, 43 and 45.

Furthermore, referring to paragraph 20-22 of the Official Action, claim 25 which is dependent on claim 24 is rejected under 35 USC §103(a) as unpatentable over Camacho further in view of US patent 6,499,089, Phelan et al (hereinafter Phelan). Phelan provides a memory with two sections being configured to allow read and write access independently of one another (see Phelan column 1, lines 25-28). The ports may access the configurable memory independently (see Phelan column 2, lines 2-33). However, combining the data ports of both terminals for being accessed by using the control port and address port of only one terminal as is claimed according to the present invention, is not disclosed or suggested by Phelan. Therefore, the subject matter of the independent claims is believed to be new and non-obvious in view of Phelan.

More particularly, with regard to dependent claim 25, this claim is also believed to be nonobvious in view of the cited references. According to claim 25 there are provided three memory areas and a third memory area of these three memory areas is assessable by the control ports and the address ports of both of the terminals, respectively, and the data to the data ports of both of the terminals, respectively. Therefore, in addition to the two memory areas, which may be accessed individually by the terminals, a third memory area is assessable by both terminals. When accessing data through both terminals, Camacho proposes to combine these terminals and to access the common RAM module (see Camacho column 8, lines 32-48). Providing a separated memory area, which allows for combined access through both terminals is not provided in Camacho. This also holds true for Phelan, wherein it is not proposed to provide a third memory area which is assessable through both terminals, whereas two other areas are accessible through the individual terminals. Therefore, it is respectfully submitted that dependent claim 25 is further not suggested by Camacho in view of Phelan.

Since each of the independent claims is believed to be allowable, all of the dependent claims are further distinguished over the cited art, including claims 25-27, 44 and 46 rejected under 35 USC §103(a).

In view of the foregoing, it is respectfully submitted that the present application as amended is in condition for allowance and such action is earnestly solicited.

Respectfully submitted,

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